A large statistics study of the performance and yields of generation-6 VLPCs (HISTE-VI)

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In this paper, the D∅ collaboration reports on the test results of over 60 000 VLPC pixels. We have explored the space of operating conditions and find good performance at a temperature of 9 K and a bias voltage of 7 V. Preliminary tests have shown an average quantum efficiency of 80% and a gain of 25,000 - 50,000. Tests have shown that the devices can be made to work at very high rates. The pixel-to-pixel variation within a chip is manageable, allowing one to assemble like-performing VLPC chips into cassettes containing 1024 pixels each.

The D∅ experiment is currently embarked on an ambitious upgrade[1] of its central tracking system. The earlier tracker has been removed and is being replaced by a super-conducting solenoid magnet, a large silicon vertex detector and an innovative tracker consisting of scintillating fibers. Each scintillating fiber is read out by an individual Visible Light Photon Counter (VLPC). These devices are solid-state photodetectors consisting of layers of doped and undoped silicon[2]. They have been previously used in much a much smaller context[3]. In the HISTE-VI model, each VLPC pixel has a 1 mm diameter circular shape, well matched for our scintillating fiber. The pixels are arranged in a 2×4 array on a chip. These chips are then soldered to an aluminum nitride substrate. The chip is connected to pads on the substrate with gold wire. These pads allow electrical access to the VLPCs. VLPC chips are epitaxially grown on 3.5” diameter wafers (176 chips/wafer). Twelve different loadings of the reactor, each containing 21 wafers, were needed to provide enough VLPCs for D∅.

Figure 1 shows typical spectra both when there is no light source present and when a weak light source illuminates a VLPC pixel. The individual photoelectron peaks are clearly evident. Even when no external light source is present, an occasional electron, dislodged by thermal processes, is observed. Because these thermal electrons are dislodged at times which are uncorrelated with the ADC gate, the average ADC signal is shifted slightly to the left. VLPCs operate at cryogenic temperatures (6-12K) and at low voltages (6-8 V). The quantum efficiency, gain and noise are all functions of these parameters, the optimum choice of which depends on the design constraints of the particular detector.

We initially show this parameter dependence by presenting the dark count rate. If one sets a threshold halfway between the zero and one photoelectron (pe) peak in the signal distribution (0.5 pe), one can plot the rate as a function of both temperature and voltage. This information is presented in figure 2. At a given voltage, the dark noise increases by approximately a factor of four per degree Kelvin. The dark count rate is a strong function of the operating voltage, increasing by a factor of 1000 over a 1.5 V span.

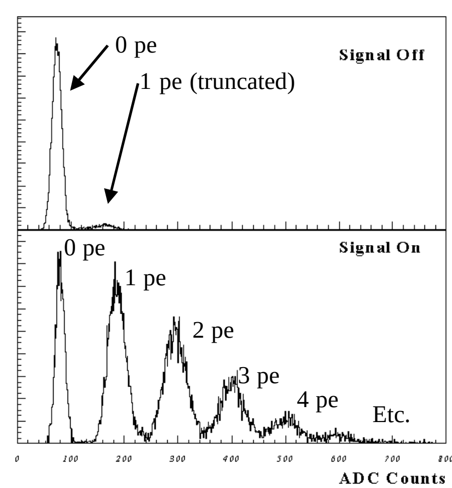

Figure 1 Typical signal distributions with and without an active light source.

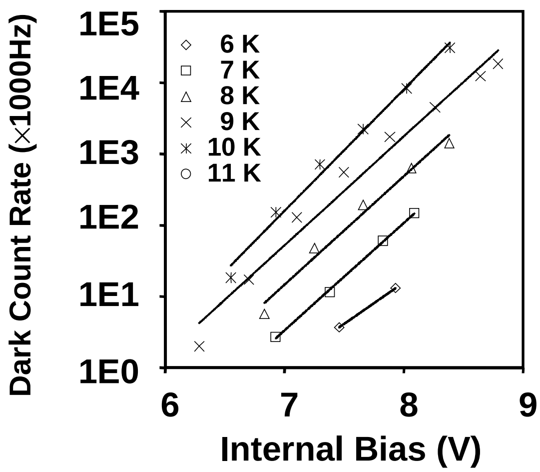

Figure 2 Dark count rate as a function of temperature and bias voltage.

An initial electron dislodged by a photon is amplified within the VLPC via a cascade mechanism inside the chip. As presented in figure 3, the gain factor is typically 30,000 – 90,000, again dependent on the bias voltage and much more weakly on the operating temperature.

The quantum efficiency (QE) of the VLPC is defined as the probability that an incident photon will dislodge an electron within the silicon and be subsequently amplified. As presented in figure 4, the QE is strongly dependent on the bias voltage until saturation. After saturation, the QE plateaus at approximately 80%. In comparison, the QE after saturation was 60% and 70% for HISTE-IV and HISTE-V respectively.

The results discussed above should be taken as typical. As we will present below, there exist moderate, but significant, variations in performance between the different reactor loads.

The results thus far presented are taken by illuminating VLPCs with an LED pulsed at low light levels and at very low rates (~ few hundreds of Hz). The environment which will be presented to the VLPCs within the D∅ detector will be much different. While the trigger rate recorded to tape will be on the order of 10-20 Hz, the charged particles that cross the scintillating fibers in uninteresting events will present the VLPCs single pe rates of 2-8 MHz (at a luminosity of 2×10^{32} cm^{-2}s^{-1}).

In order to test the response of the VLPCs at higher background rates, VLPCs were illuminated by two LEDs, one pulsing at a fast rate, the other at a rate representative of triggers. Figure 5 shows the relative QE (R_{QE}) [R_{QE} = QE(High Rate) /QE (Low Rate)] and gain as a

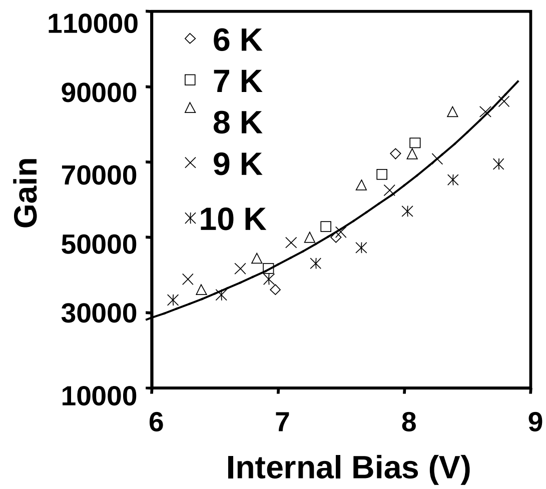

Figure 3 Gain of VLPCs as a function of temperature and bias voltage.

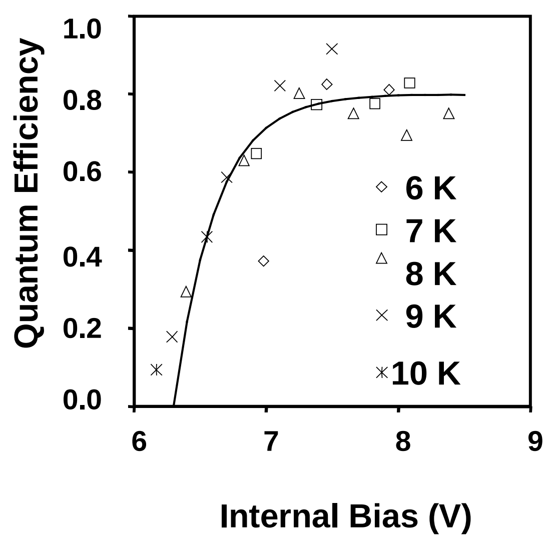

Figure 4 Quantum efficiency as a function of temperature and bias voltage.

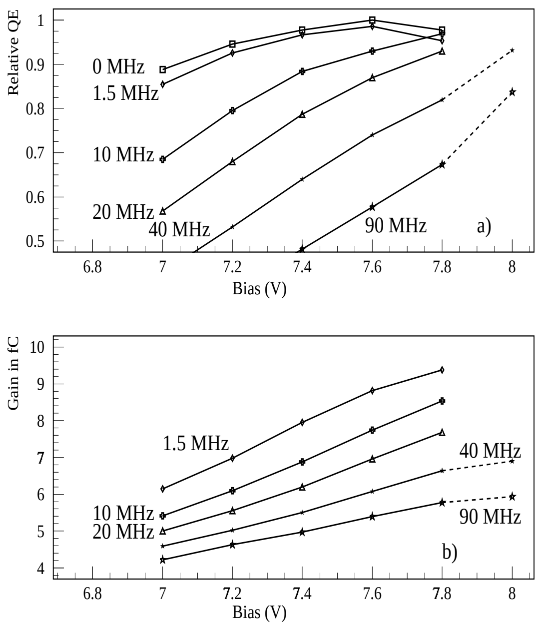

Figure 5 (a) Relative QE and (b) gain in fC (note 1 fC = a gain factor of ×6250) as a function of background rate. Both figures are taken to be representative in structure and show data from reactor load 737.

function of bias voltage and background pe rate. As observed from the figure, the normalization point is 7.6 V at a background rate of 0 MHz. This voltage is the point at which the efficiency is maximized (discussed below).

While the VLPC performance is degraded by the presence of a high pe background rate, one may recover this performance by slightly increasing the operating voltage. For a background rate of 20 MHz, this increase needs to be about 0.5 V. A more detailed discussion of these results is given in reference 4.

The D∅ detector will need approximately 100,000 VLPC pixels for its Run II upgrade. The VLPCs will be organized into approximately 100 cassettes, each containing 1024 pixels. For ease of operation and triggering, it is necessary to sort the VLPCs into like-operating groups. Consequently, each chip is tested before assembly.

Fourteen chips are place in a cryostat and cooled to 9K. While it would be possible to operate individual cassettes at different temperatures, the simplicity of single temperature operation was an attractive and natural choice. The VLPCs are illuminated by two LEDs (signal and background). The background rate is initially set to zero and the signal LED is calibrated. This removes errors incurred by each opening, reloading and reassembly of the cryostat. The background LED is then strobed at 10 MHz, with an average number of pe of 2 (20 MHz single pe equivalent). Data is then taken both with and without the signal pulser on. The operating voltage of the VLPC is increased in 0.2 V increments until a voltage is found which maximizes the single fiber hit efficiency expected in the D∅ environment.

This efficiency is determined by the following method. Because the fiber tracker will form the backbone of the tracking trigger, one must set a threshold above which a fiber will be considered hit. The desire for high efficiency must be balanced against the desire for a low accidental rate. Using a signal distribution without illumination from the signal LED, but with the background LED on, one sets a threshold which the VLPC signal exceeds only 0.5% of the time.

The gain of each pixel is determined by fitting the signal distribution (see figure 1b) to four gaussians and determining the separation between the one and two pe peaks. The average number of pe's is determined by dividing the average signal above pedestal by the gain. The average signal was arbitrarily set to be approximately 1.5 pe to ensure the distributions could be easily fitted.

Earlier measurements[5] have shown that a detector consisting of 3HF scintillating fiber and VLPCs will have an average signal of 9 pe per minimum ionizing particle crossing the fiber at normal incidence. Thus we scale the incident light of each pixel to 9 pe and include a factor which accounts for the light yield measured by the calibration VLPC.

$$\text{Signal(scaled)} = \frac{9.0}{\text{Signal(calibration)}} \times \text{Signal(observed)}$$

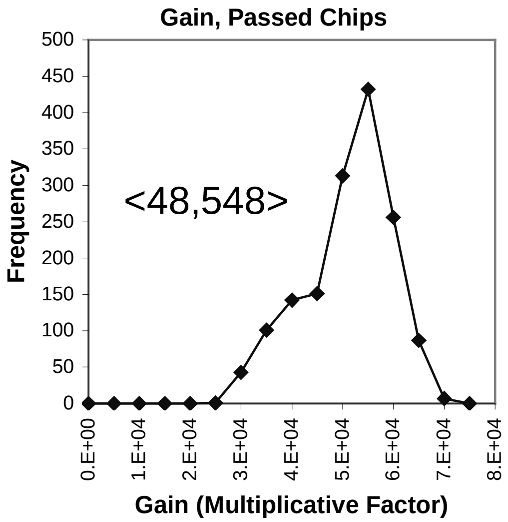

Figure 6 Gain distribution of chips from reactor load 735.

Reactor Load	<Gain> x1000	RMS Gain x1000	# Passed Chips
733	45.2	7.5	1736
735	48.5	8.6	1533
737	48.6	6.5	221
739	38.3	6.6	260
1154	39.5	3.1	47
1162	37.6	6.9	467
1164	31.1	5.5	1652
1166	34.1	7.4	772
1168	25.6	4.1	116
1170	26.0	5.1	116
1172	34.6	4.8	407
1174	29.9	6.5	262

Table 1 Mean and RMS gain for different reactor loads. Because the testing of chips is ongoing, not all reactor loads have been equally sampled.

The efficiency is then calculated using the measured threshold and the scaled response. This calculation is accomplished using conventional Poisson statistics, although a small correction is added to account for the width of the individual pe peaks.

The efficiency of a chip is defined to be the average of the efficiency of its eight pixels. A

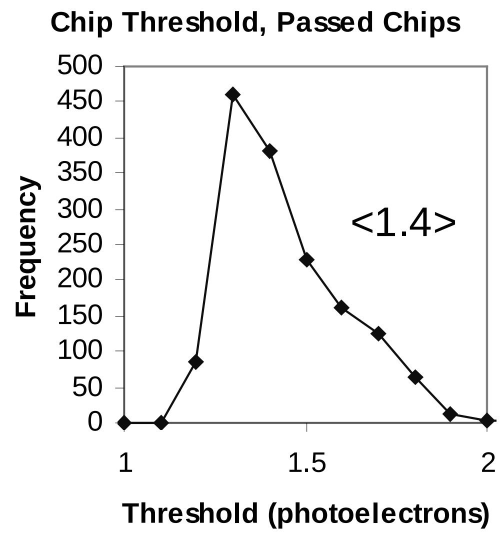

Figure 7 Distribution of thresholds in units of photoelectrons. While the distribution is restricted to reactor load 735, the others are quite similar.

chip is considered acceptable if there is a voltage for which all of its pixels have an efficiency exceeding 99%.

A test is applied at each voltage where the average gain of the 6 pixels with highest gain is calculated. If any of the pixels have a gain which is less than 80% of this mean, then the voltage is considered to be unacceptable for this chip. The voltage is varied until a maximum efficiency is found, subject to the above mentioned constraints. For higher voltages (typically 0.5-1.0 V above the optimum), the chips undergo a ‘breakdown’ mode, characterized by large electrical discharges. Typically 85% of tested chips pass the testing criteria.

Figure 6 shows the gain distribution for chips from a particular reactor load. The average gain is quite high (48,500) with an RMS of 8,600. Not all reactor loads have the same average gain. Table 1 shows the spread of average gain for these different growth cycles. The cause of this variation is unknown, as the vendor (Boeing

N.A.) made every effort to produce identical devices.

The 0.5% noise trigger threshold can be presented in two ways. The first is simply in units of photoelectrons. Figure 7 shows the distribution for passed chips. The average of 1.4 is independent of reactor load and is well below the estimated yield of 9 pe/MIP in the fiber tracker. (Note 9 pe/MIP was determined using HISTE-IV. The improved QE of HISTE-VI is expected to increase this yield to 12 pe.) Because D∅'s trigger electronics set thresholds on total charge, the pe threshold is not the entire story. One must multiply the pe threshold by the gain and convert to charge. Figure 8 shows the distribution of thresholds in these units for a particular reactor load. Other reactor loads have average thresholds which reflect the gain variations. The minimum threshold which can be set is approximately 3.5 fC.

Because the D∅ trigger architecture provides a single trigger threshold to a particular chip, the threshold variation within a chip is of interest.

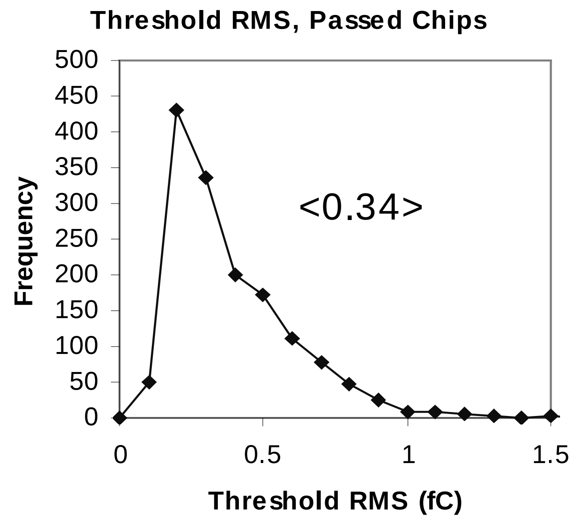

Figure 9 Distribution of RMS' of VLPC threshold in units of fC. The RMS is of the 8 pixels within each chip. Presented distribution is limited to reactor load 735.

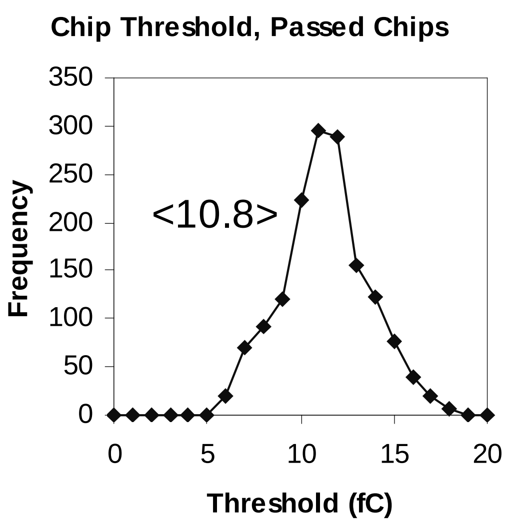

Figure 8 Distribution of thresholds in units of femtocoulombs. Presented distribution is limited to reactor load 735.

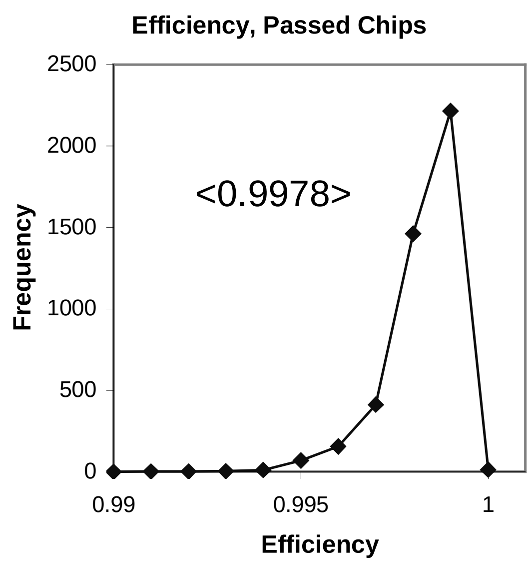

Figure 10 Distribution of single-fiber, single-MIP efficiencies expected in the D∅ detector. This result is determined by the data presented here in conjunction with the light yield measured earlier.

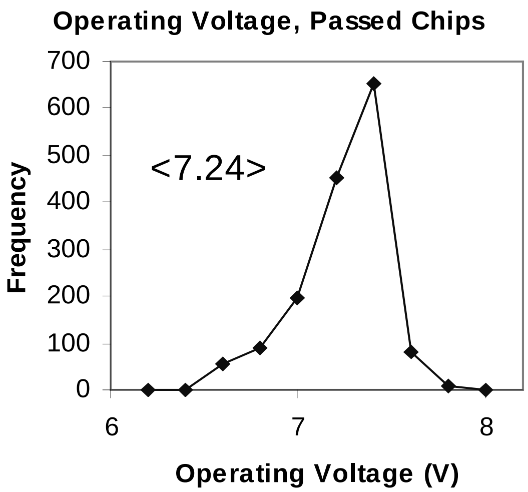

Figure 11 Distribution of operating voltage for passed chips. Presented distribution includes only chips from reactor load 735.

One may calculate the RMS of the thresholds for the 8 pixels contained within a chip. Figure 9 shows the distribution of threshold RMS. The very low RMS demonstrates that within a chip the noise characteristics are quite similar.

Figure 10 shows the distribution of single-fiber, single-MIP efficiencies. The distribution is clearly unaffected by the requirement that the chip efficiency exceeds 99%.

Because the performance of the VLPC is very dependent on the bias voltage, if one wishes to supply a single voltage to a cassette, it is necessary to group VLPCs with identical operating voltages. The optimum operating voltage varies significantly among the different reactor loads, although within a reactor load the variation is much reduced. Figure 11 shows the distribution of optimum operating voltages for a particular reactor load. Mean and RMS operating voltages are shown in Table 2 for the different reactor loads.

Thus the D∅ experiment has measured the performance characteristics of a large number of

Reactor Load	Mean Voltage	RMS Voltage
733	6.87	0.24
735	7.24	0.23
737	7.23	0.37
739	6.80	0.25
1154	6.52	0.11
1162	6.38	0.21
1164	7.03	0.23
1166	6.63	0.24
1168	6.71	0.20
1170	6.27	0.21
1172	7.20	0.18
1174	6.94	0.24

Table 2 Variation in optimum operating voltage for the different reactor loads.

VLPCs. The very high quantum efficiency (80%) is essentially of wavelength independent (at the factor of two level) across the visible spectrum. The gain depends on parameters, such as operating voltage and temperature, but typically is in the range of 25,000 – 50,000. The noise characteristics are very attractive, with noise rates in the range of 10-100 kHz, under reasonable operating conditions. The VLPC has proven itself to be an impressive photodetector and will be an attractive choice for any scintillating fiber detector.

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[1]S. Abachi et al., FERMILAB-PUB-96-357-E.
[2]G.B. Turner et al., proceedings of SCIFI93, 1995; M.G. Stapelbroek and M.D. Petroff, ibid.
[3]M. Ambrogiani et al., IEEE Trans. Nucl. Sci. 44 (1997) 460; R. Mussa et al., Nucl. Instrum. Meth. A 360 (1995) 13.
[4]A. Bross et al., '*VLPC Characterization*', to be published in the proceedings of SciFi '97.
[5]D. Adams et al., Nucl. Phys. Proc. Suppl., 44 (1995) 332.